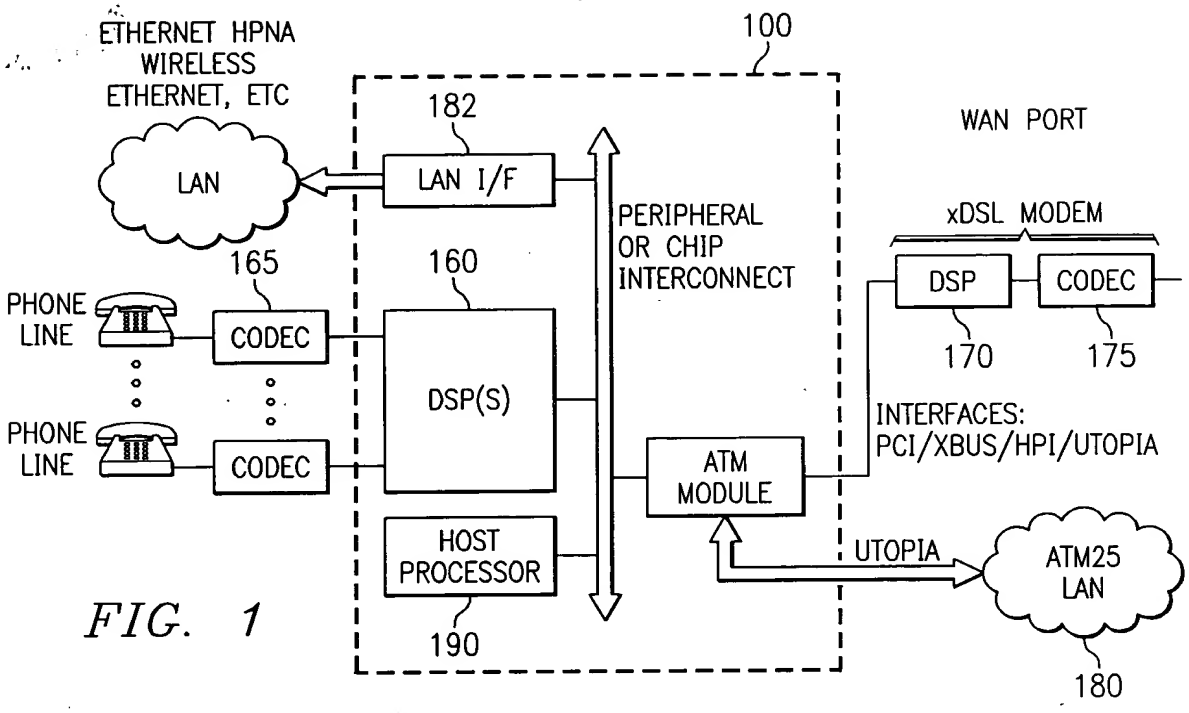
ETHERNET HPNA
WIRELESS
ETHERNET, ETC
LAN
182
LAN I/F
100
WAN PORT
xDSL MODEM
DSP
CODEC
170
175
PERIPHERAL
OR CHIP
INTERCONNECT
165
160
PHONE
LINE
CODEC
DSP(S)
PHONE
LINE
CODEC
INTERFACES:
PCI/XBUS/HPI/UTOPIA
ATM
MODULE
HOST
PROCESSOR
UTOPIA
ATM25
LAN
190
180

FIG. 1

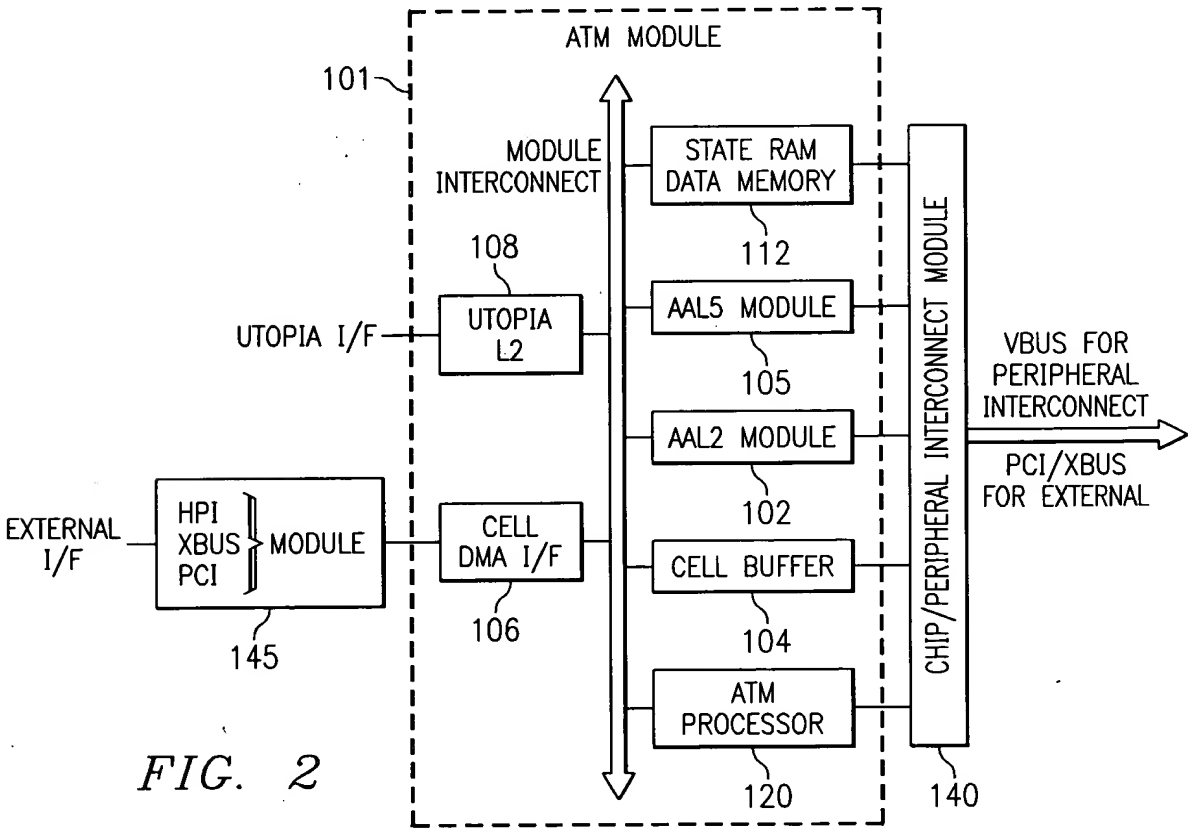
ATM MODULE
101
MODULE
INTERCONNECT
STATE RAM
DATA MEMORY
112
108
UTOPIA I/F
UTOPIA
L2
AAL5 MODULE
105
AAL2 MODULE
VBUS FOR
PERIPHERAL
INTERCONNECT
PCI/XBUS
FOR EXTERNAL
102
EXTERNAL
I/F
HPI
XBUS
PCI
MODULE
CELL
DMA I/F
CELL BUFFER
104
106
ATM
PROCESSOR
CHIP/PERIPHERAL INTERCONNECT MODULE
145
120
140

FIG. 2

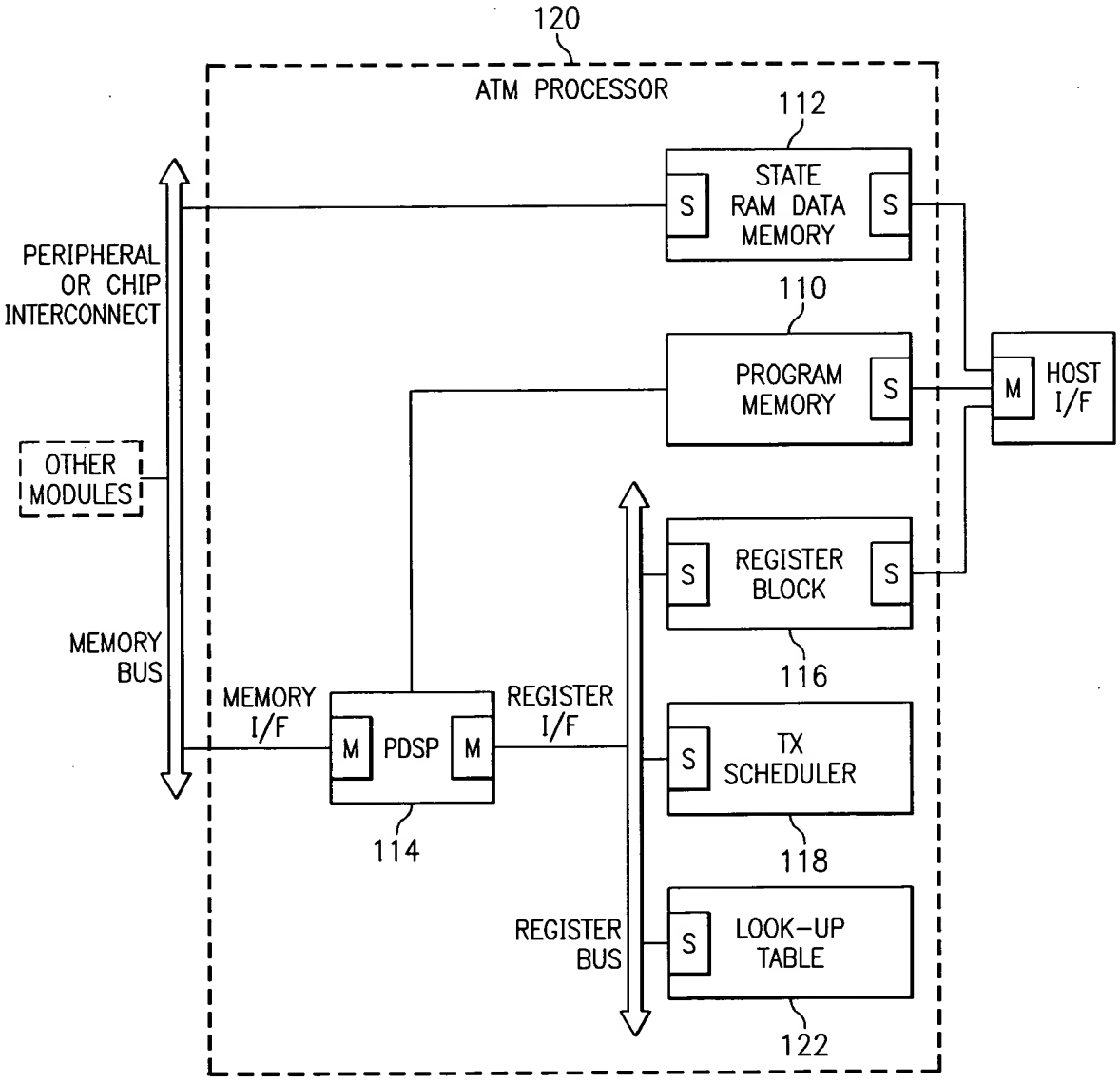
120
ATM PROCESSOR
112
STATE RAM DATA MEMORY
S
S
PERIPHERAL OR CHIP INTERCONNECT
110
PROGRAM MEMORY
S
M
HOST I/F
OTHER MODULES
REGISTER BLOCK
S
S
MEMORY BUS
116
MEMORY I/F
M
PDSP
M
REGISTER I/F
TX SCHEDULER
S
114
118
REGISTER BUS
LOOK-UP TABLE
S
122

FIG. 3

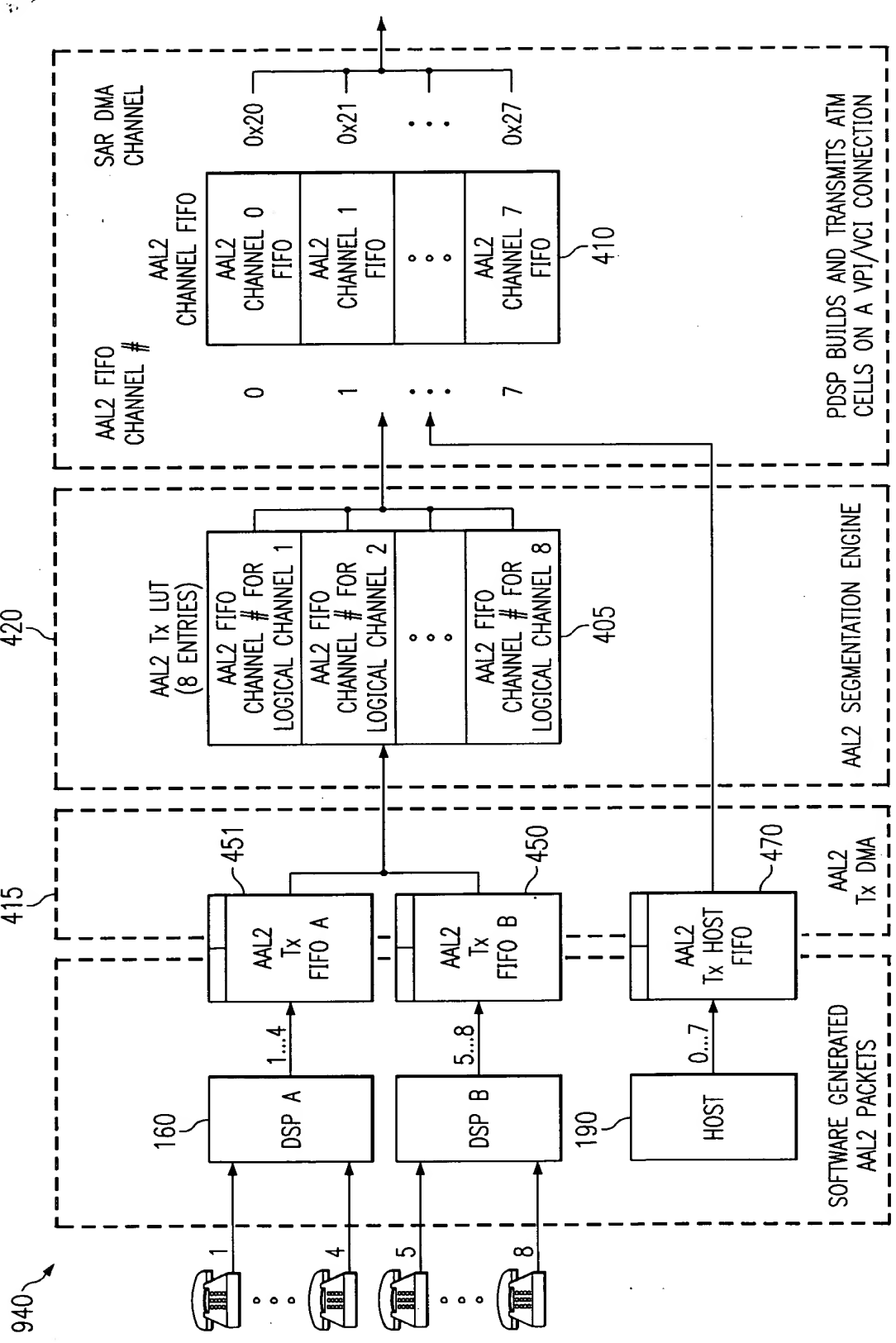
SAR DMA CHANNEL
AAL2 FIFO CHANNEL #
AAL2 CHANNEL FIFO
AAL2 CHANNEL 0 FIFO
AAL2 CHANNEL 1 FIFO
AAL2 CHANNEL 7 FIFO
410
0x20
0x21
0x27
0
1
7
PDSP BUILDS AND TRANSMITS ATM CELLS ON A VPI/VCI CONNECTION
420
AAL2 Tx LUT (8 ENTRIES)
AAL2 FIFO CHANNEL # FOR LOGICAL CHANNEL 1
AAL2 FIFO CHANNEL # FOR LOGICAL CHANNEL 2
AAL2 FIFO CHANNEL # FOR LOGICAL CHANNEL 8
405
AAL2 SEGMENTATION ENGINE
415
451
450
470
AAL2 Tx FIFO A
AAL2 Tx FIFO B
AAL2 Tx HOST FIFO
AAL2 Tx DMA
1...4
5...8
0...7
160
DSP A
DSP B
190
HOST
SOFTWARE GENERATED AAL2 PACKETS
940
1
4
5
8

FIG. 4

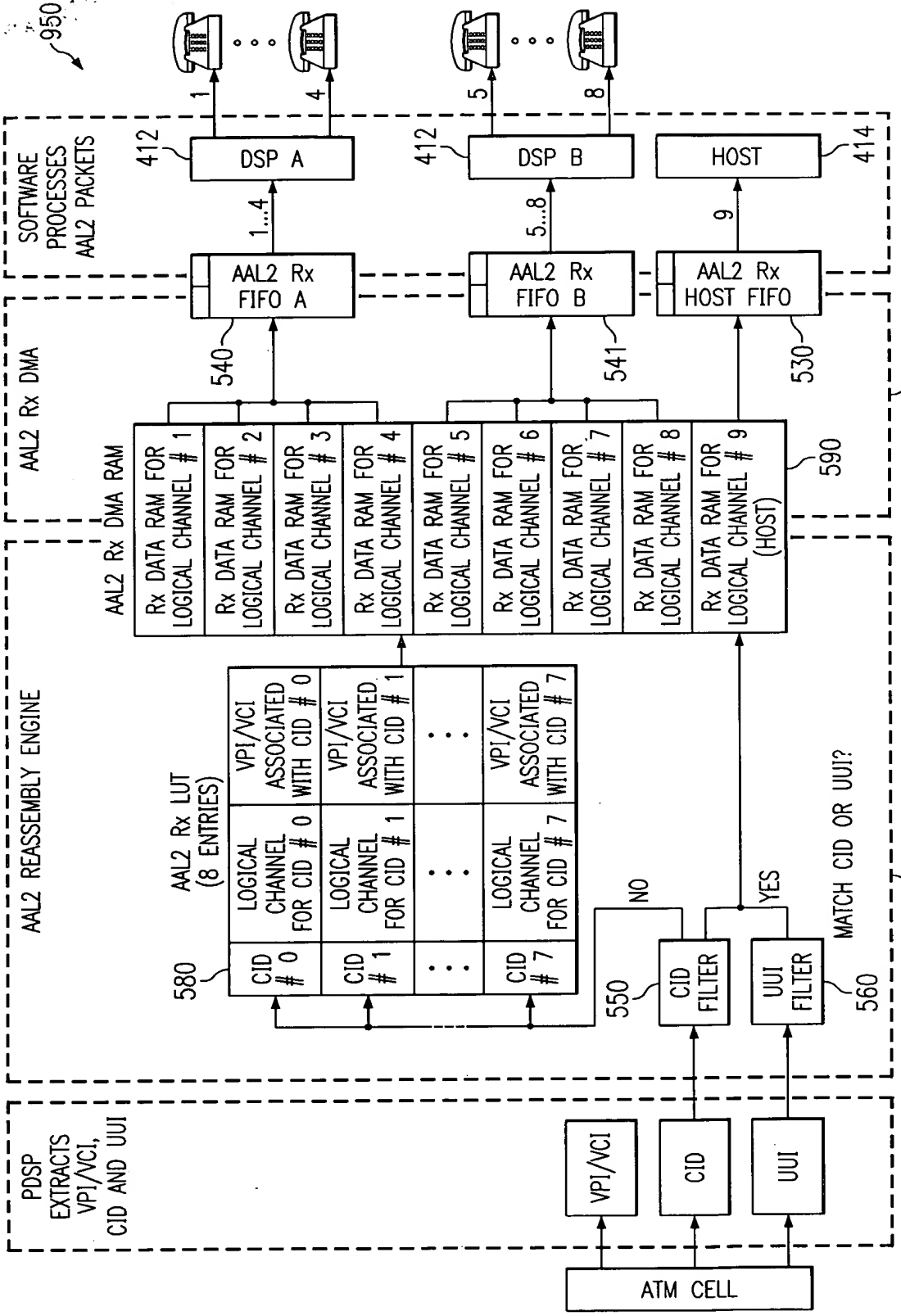
950
1
4
5
8
412
DSP A
412
DSP B
HOST
414
SOFTWARE PROCESSES AAL2 PACKETS
1...4
5...8
9
AAL2 Rx FIFO A
AAL2 Rx FIFO B
AAL2 Rx HOST FIFO
540
541
530
515
AAL2 Rx DMA
AAL2 Rx DMA RAM
Rx DATA RAM FOR LOGICAL CHANNEL # 1
Rx DATA RAM FOR LOGICAL CHANNEL # 2
Rx DATA RAM FOR LOGICAL CHANNEL # 3
Rx DATA RAM FOR LOGICAL CHANNEL # 4
Rx DATA RAM FOR LOGICAL CHANNEL # 5
Rx DATA RAM FOR LOGICAL CHANNEL # 6
Rx DATA RAM FOR LOGICAL CHANNEL # 7
Rx DATA RAM FOR LOGICAL CHANNEL # 8
Rx DATA RAM FOR LOGICAL CHANNEL # 9 (HOST)
590
AAL2 REASSEMBLY ENGINE
AAL2 Rx LUT (8 ENTRIES)
CID # 0
CID # 1
CID # 7
LOGICAL CHANNEL FOR CID # 0
LOGICAL CHANNEL FOR CID # 1
LOGICAL CHANNEL FOR CID # 7
VPI/VCI ASSOCIATED WITH CID # 0
VPI/VCI ASSOCIATED WITH CID # 1
VPI/VCI ASSOCIATED WITH CID # 7
580
NO
YES
550
CID FILTER
UUI FILTER
560
MATCH CID OR UUI?
520
PDSP EXTRACTS VPI/VCI, CID AND UUI
VPI/VCI
CID
UUI
ATM CELL

FIG. 5

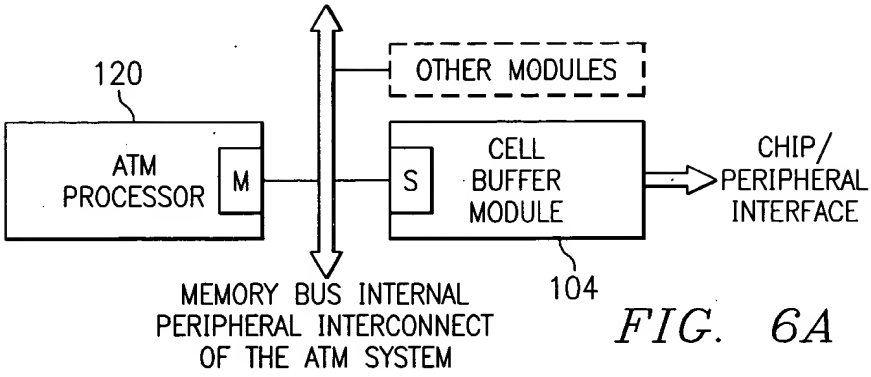

FIG. 6A

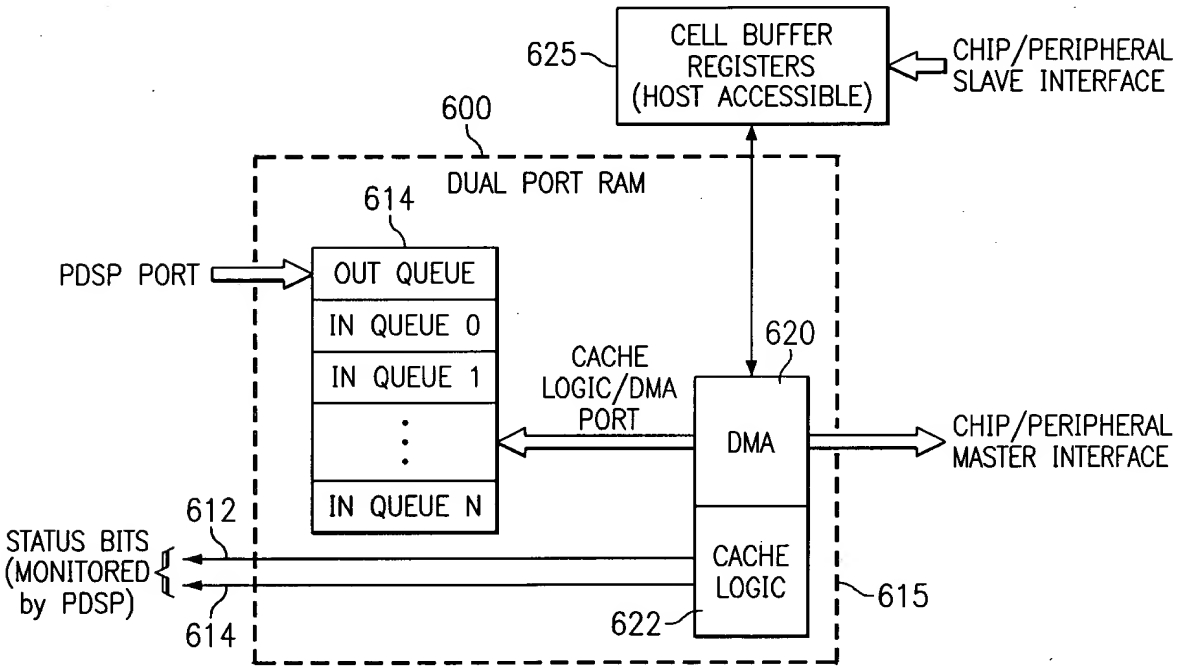

FIG. 6B

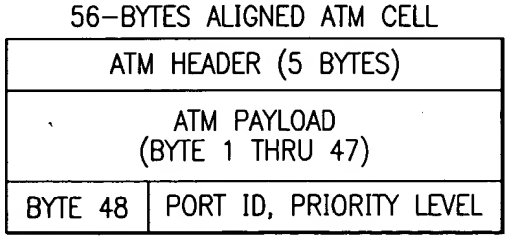

FIG. 7

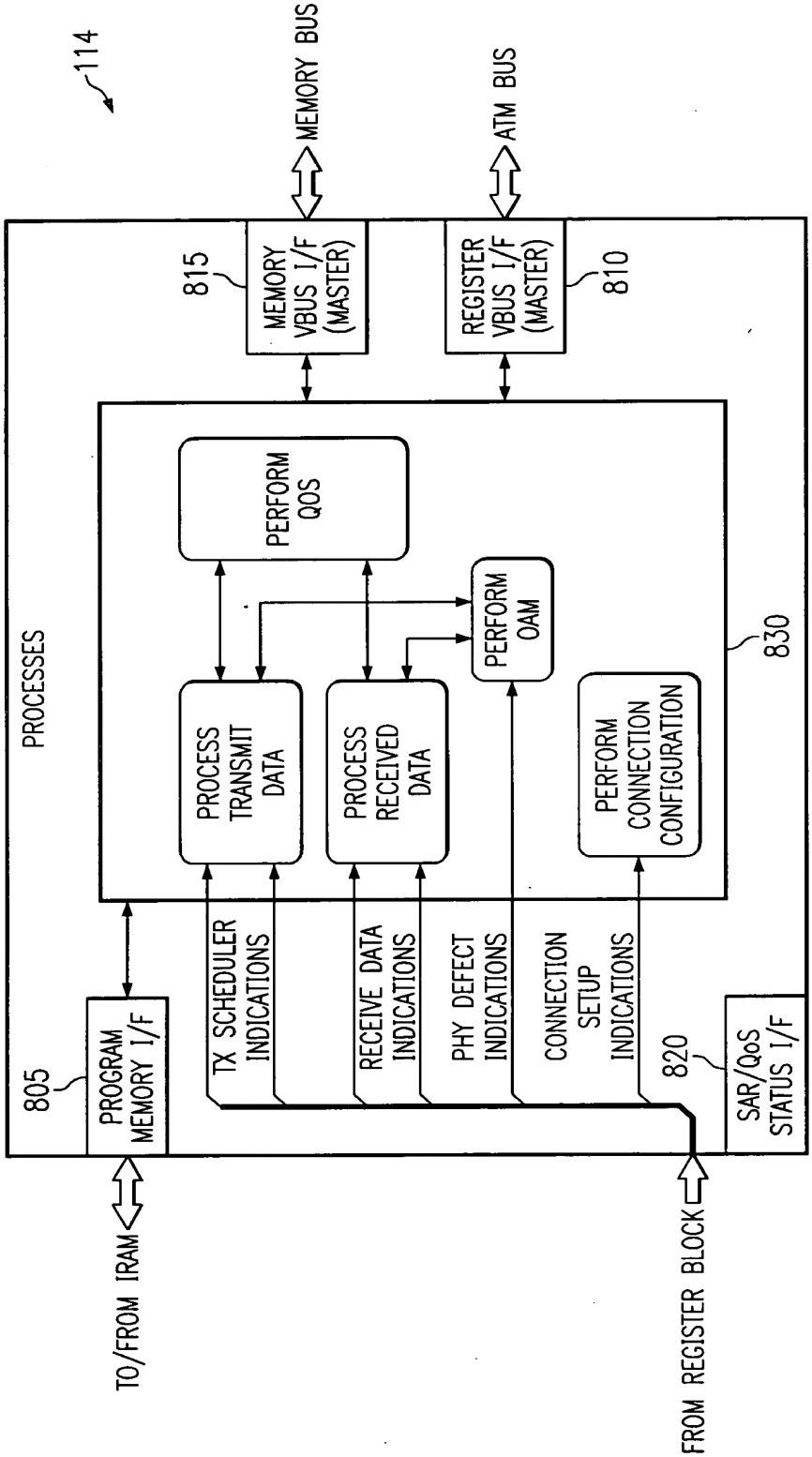
114
MEMORY BUS
ATM BUS
815
MEMORY VBUS I/F (MASTER)
REGISTER VBUS I/F (MASTER)
810
PROCESSES
PERFORM QOS
PERFORM OAM
PROCESS TRANSMIT DATA
PROCESS RECEIVED DATA
PERFORM CONNECTION CONFIGURATION
830
805
PROGRAM MEMORY I/F
TX SCHEDULER INDICATIONS
RECEIVE DATA INDICATIONS
PHY DEFECT INDICATIONS
CONNECTION SETUP INDICATIONS
820
SAR/QoS STATUS I/F
TO/FROM IRAM
FROM REGISTER BLOCK

FIG. 8